EVOLUTION CAPITAL

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Efficiency at Its Finest: The Next-Gen of AI Chips

Evolution Capital initiates coverage on Nanoveu (ASX:NVU) with a fair value of A$0.26 per share, representing significant upside to the current market price. Nanoveu is entering a new commercial phase, following the completion and tape-out (design sent for fabrication) of its ECS-DoT chip – a purpose-built ultra-low power AI processor that targets the fast-growing edge computing (local on-device processing) market.

After years of deep technical development and engineering investment, the ECS-DoT chip is now real – fully designed, validated, and sent to TSMC for fabrication. This milestone transforms Nanoveu from a concept-stage fabless chip developer into a revenue-generating commercial opportunity. Developer Kits have already been shipped to customers, enabling early engagement with OEMs and system integrators across drone, IoT, and embedded device markets. In a recent real-world field test, ECS-DoT extended the flight time of a battery-powered drone by more than 33% – a striking proof point of its ultra-efficient power consumption and a clear demonstration of competitive advantage in battery-sensitive environments.

An Ultra-Efficient Chip Built for the Edge AI Boom

The ECS-DoT is engineered to run AI workloads directly on devices– a growing need as latency, privacy, and power constraints push computing away from the cloud and toward the edge. The current version of the chip is designed on TSMC's 22nm node, with the next gen chip moving to TSMC's 16nm FinFET node. The chip combines low power draw, fast local inference, and cost-efficient scalability. Its architecture has been optimised for sparse computing and vision-centric AI tasks, enabling advanced features like object detection and gesture recognition on tiny batteries – without needing to constantly transmit data.

Nanoveu's model centres on getting ECS-DoT into customers' hands through Developer Kits and converting those engagements into ultimately, high-volume chip sales. As a fabless company, Nanoveu leverages external foundries for manufacturing, keeping capital intensity low while retaining control over design and IP. In parallel, the company is building a recurring revenue stream through software-enabled customisation and design services, aligning with customer needs over multiple product cycles.

From Engineering Success to Commercial Momentum

With the current chip now sampling to OEM customers, Nanoveu is entering the early stages of commercial engagement. Initial Developer Kits have shipped, and partners across drones, robotics, and wearables are already trialling the ECS-DoT chip. Its adaptable architecture supports a wide range of vision AI use cases, enabling lightweight intelligence on the edge.

The market for edge AI is rapidly expanding as industries move toward on-device processing to improve latency, efficiency, and battery life. Nanoveu's power-efficient and cost-effective chip positions it well to capitalise on this trend.

With a fully developed chip, growing customer interest, and a lean, capital-light model, Nanoveu offers an attractive pre-scale opportunity. The next 12–18 months will be pivotal, as customer trials convert to design wins and commercial orders – potentially unlocking a long-term growth story.

Key Near-Term Catalysts	
Initial DevKit evaluations convert into signed design wins with OEMs	CY25–CY26
First commercial volume shipments of ECS-DoT chip to early customers	From CY26
Execution of new engineering contracts with commercial partners	Ongoing
Developer Kit distribution expands across additional verticals (e.g., robotics, wearables)	CY25–CY26
Strategic partnership or JV agreement with major industry player	CY25–CY26

Recommendation	**Spec Buy**
Share Price	**$0.08**
Fair Valuation	**$0.26**

Company Profile	
Market Cap	$75M
Enterprise Value	$70M
Free Float	66%
Cash	$4.5m
52-Week Range	$0.018 - $0.083

Price Performance

Company Overview

Nanoveu is an Australian semiconductor company focused on ultra-efficient edge AI solutions for vision-based applications. Its flagship ECS-DoT chip brings real-time, low-power intelligence directly onto devices, reducing reliance on the cloud, cutting latency, and extending battery life by up to one-third. Designed for high-growth markets such as drones, robotics, smart cameras, and wearables, ECS-DoT combines a vision-optimised architecture with exceptional energy efficiency, enabling advanced AI capabilities in products where weight, size, and power constraints are critical. Operating under a capital-light, fabless model with manufacturing outsourced to leading foundries like TSMC, Nanoveu concentrates on design, proprietary IP, and customer integration, while its legacy Nanoshield and EyeFly3D products continue to provide supporting revenue as the chip business scales to become its primary growth engine.

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Investment Case

A Company in Transition: From Specialty Films to AI Silicon

Nanoveu Ltd (ASX: NVU) is undergoing a strategic transformation. Formerly known for antiviral surface coatings (Nanoshield™) and glasses-free 3D screen technology (EyeFly3D), the company pivoted sharply in late 2024 with the acquisition of EMASS Pte Ltd, bringing proprietary semiconductor IP in-house and repositioning NVU as a deep-tech hardware platform.

At the core of this shift is ECS-DoT, Nanoveu's ultra-low-power AI system-on-chip (SoC). Built on a 32-core RISC-V architecture, ECS-DoT delivers real-time inference for edge applications at power levels below 1 mW, enabling AI to run locally on drones, wearables, healthcare devices, and industrial systems without reliance on cloud infrastructure or excessive energy consumption.

With this architecture, Nanoveu directly enters one of the fastest-growing segments in semiconductors: on-device intelligence, also known as Edge AI.

While Nanoveu's transition into edge AI hardware is gaining traction, the core of the investment case ultimately rests on three key questions that investors should be asking. These questions not only define the opportunity, but also help frame how execution, differentiation, and valuation could evolve from here:

1. How big is Nanoveu's opportunity in the global Edge AI wave?
2. What makes ECS-DoT different - and defensible?
3. Where does the valuation go from here - 2x, 3x, or more?

Strategic Valuation with Room to Re-Rate

At a current market capitalisation of ~A$60 million (as of July 2025), Nanoveu is no longer a hidden microcap, but it remains modestly valued relative to peers in the low-power AI hardware space. Global players like Kinara, Syntiant, and Ambiq have raised or exited at significantly higher valuations, often with less public technical validation and weaker market timing.

What differentiates Nanoveu is its execution visibility:

- ECS-DoT has already demonstrated performance benefits in drone simulations (e.g. +33% flight time)
- Developer kits with the current 22nm chip are already sampling to OEM customers
- A new modular developer kit is set to launch in Q3 2025
- The next version of the chip is ready for 16nm tape-out at TSMC in Q4 2025
- OEM discussions are underway, targeting first integration deals by early 2026

While the market has started to re-rate Nanoveu, the share price still reflects legacy perceptions tied to coatings and display tech, not the upside from a scalable, IP-driven semiconductor business.

Upcoming Catalysts (2025–2026)

Nanoveu is entering a critical phase, with multiple near-term milestones that could materially shift market perception.

The company has developer kits built around its ECS-DoT chip already sampling to customers, with a new modular version coming in Q3 2025. Targeted at drones, wearables, and IoT systems, the kit allows OEMs to test ECS-DoT in real-world conditions — a key step toward adoption.

By Q4 2025, the next version of the ECS-DoT is scheduled for tape-out on TSMC's 16 nm process node, advancing the chip to a smaller, more efficient architecture. This upgrade will enhance performance, lower power consumption and reduce die size, providing a stronger platform for commercial engagements.

Also in H2 2025, Nanoveu will publish results from its Phase-2 drone trials, which aim to demonstrate real energy savings and AI performance in live flight conditions. Early simulations showed up to 33% longer battery life.

Looking ahead to early 2026, the company is targeting its first OEM partnerships, followed by initial product-based revenue from ECS-DoT in H2 2026. These steps would mark Nanoveu's transition from R&D to early-stage commercialisation.

Nanoveu is one of the few ASX-listed companies offering pure-play exposure to edge AI silicon, and the timing is right.

For investors, the opportunity lies in the combination of IP, execution, and timing. The valuation has moved beyond pre-commercial levels but does not yet fully reflect the platform's potential.

Company Overview

Business Model & Segment Focus

Nanoveu Ltd (ASX: NVU) is an Australian technology company operating at the intersection of semiconductor design, advanced visualisation, and functional surface coatings. Since its strategic repositioning in late 2024, the company has restructured around three core business segments — each targeting high-growth, innovation-driven markets:

1. EMASS – Ultra-Low-Power AI Semiconductors: Design and development of proprietary system-on-chip (SoC) architectures optimized for edge AI applications. ECS-DoT, the flagship chip, is built on a RISC-V framework and leverages ReRAM-based neural compute for real-time inference at sub-milliwatt power levels.

2. EyeFly3D – Autostereoscopic Display Solutions: A software- and hardware-based 3D rendering platform that enables glasses-free depth perception on mobile displays. Future integration of ECS-DoT will allow local, AI-powered depth mapping and content adaptation in real time.

3. Nanoshield™ – Functional Surface Coatings: A proprietary film infused with cuprous nanoparticles designed to deliver antiviral, antimicrobial, and anti-fouling protection. Applications include solar panel coatings, marine infrastructure, and consumer devices.

Strategic Focus and Technology Platform

Since acquiring EMASS, Nanoveu has shifted its focus decisively toward commercialising its edge AI semiconductor platform. At the heart of this strategy is the ECS-DoT chip – a custom-built system-on-chip designed for real-time AI processing in devices where power budgets and physical space are severely limited.

The target applications span a broad range: drones that need to navigate autonomously without draining their batteries, healthcare wearables that must continuously monitor and analyse vital signs, industrial automation systems that run AI on-site, and other

embedded control systems where cloud connectivity isn't always practical or fast enough.

Technically, ECS-DoT is built around a 32-bit RISC-V architecture co-integrated with a dedicated hardware accelerator for AI applications, chosen for its openness and flexibility. It is designed for ultra-low-power operation, minimal heat output, and instant response times – key attributes for edge devices. The chip can accommodate AI models with up to 13 million parameters, fully stored on-chip without any need for external memory, and has demonstrated more than 30 GOPS (Giga Operations per Second) per watt in benchmark tests. This performance positions ECS-DoT as a compelling alternative to bulkier, power-hungry legacy processors like GPUs (graphics processing units) and NPUs (neural processing units) when it comes to small, battery-powered products.

While Nanoveu's legacy businesses remain active, the company's core value creation going forward will come from its semiconductor division. The older product lines – EyeFly3D (glasses-free 3D technology) and Nanoshield™ (protective and solar coatings) – still hold commercial potential and share synergies with the ECS-DoT platform. EyeFly3D, for example, could ultimately leverage on-device AI processing to enhance user experiences, while Nanoshield™ coatings are currently in trials for renewable energy and large-scale infrastructure projects, potentially benefiting from the same AI-driven sensing and control capabilities that ECS-DoT enables.

Platform Focus: EMASS & ECS-DoT SoC

SoC Architecture: RISC-V, ReRAM, AI Acceleration

Nanoveu's semiconductor subsidiary EMASS has developed a proprietary system-on-chip (SoC) platform called ECS-DoT, which forms the foundation of the company's move into edge AI – artificial intelligence that runs directly on devices rather than being sent off to the cloud. This shift is crucial for products where every milliwatt of power and every millisecond of latency matters – think drones, wearables, or medical sensors – devices that need to be small, battery-efficient, and instantly responsive.

At the heart of ECS-DoT is a lightweight RISC-V CPU core, which manages and coordinates the chip's dedicated deep-learning accelerators. These custom AI engines handle the heavy lifting for neural network inference, while the RISC-V core orchestrates dataflow and system tasks. Unlike proprietary architectures like ARM, RISC-V is open and license-free, allowing EMASS to tailor the instruction set and micro-architecture specifically for ultra-low-power AI workloads, without incurring expensive licensing fees.

A defining feature of ECS-DoT is its use of on-chip non-volatile memory, such as MRAM (Magnetoresistive Random Access Memory) or ReRAM (Resistive Random Access Memory), as ultra-low-power local storage. Instead of constantly pulling data from large external memories, ECS-DoT keeps AI weights and key data locally on-chip, dramatically reducing energy use and latency. This compact design eliminates the need for external DRAM and enables ECS-DoT to deliver always-on AI processing in a sub-milliwatt power envelope.

The chip also integrates dedicated AI acceleration units – specialized hardware designed to handle the heavy lifting for modern AI tasks, from image recognition to natural language processing. These accelerators are built for repetitive, data-intensive jobs – like a fitness band continuously analysing heart rate data, or an industrial camera spotting defects on a production line.

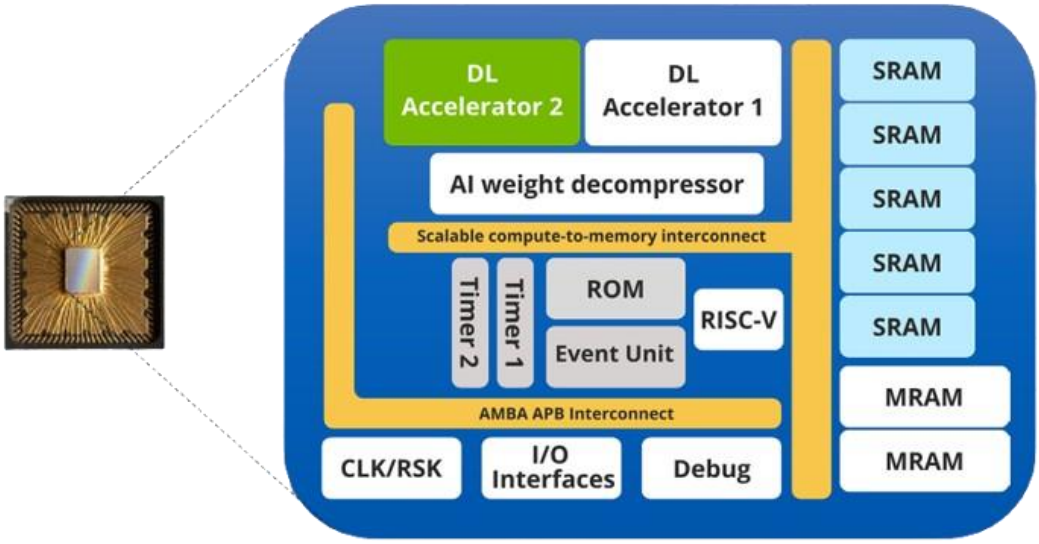
ECS-DoT's architecture is designed for flexibility rather than one-size-fits-all integration. Its RISC-V control core, dedicated AI accelerators and on-chip memory are paired with a wide I/O matrix (I^2C, SPI, UART, etc.), allowing product makers to connect the sensors and radios they need, whether that's cameras for drones or biometric inputs for wearables. The chip's ultra-low-power design selectively powers down unused blocks,

enabling always-on AI without draining the battery, a critical feature for devices like medical wearables and IoT nodes.

In short, ECS-DoT tackles the biggest challenges of on-device AI: limited energy, limited space, and limited compute power. EMASS has combined open, cost-efficient RISC-V cores, cutting-edge ReRAM memory, and AI accelerators into a compact, customizable chip.

This makes ECS-DoT highly attractive for companies looking to embed intelligence directly into their products – from smart home devices and industrial sensors to wearables and autonomous drones – without the delays, costs, and power drain of cloud-based processing.

Figure 1: ECS-DoT chip architecture



Source: Nanoveu Investor Webinar, 9 July 2025, Slide 9.

Performance Metrics (GOPS, Power, Parameters)

The ECS-DoT chip was developed with a clear goal: to deliver top-tier AI performance in devices that operate under strict constraints for power, size, and heat. Whether embedded in a drone, a wearable, or a medical device, ECS-DoT is designed to run real artificial intelligence applications efficiently and reliably on-device.

In internal testing, ECS-DoT achieves over 30 GOPS per watt of computing performance. GOPS stands for "Giga Operations Per Second," meaning billions of calculations every second. The "per watt" figure shows how much power is needed for that performance – and ECS-DoT sits well above industry averages for battery-powered chips. In practical terms, this means that in a smartwatch or sensor, ECS-DoT can execute billions of operations while drawing less than a single milliwatt of power.

The chip operates in an ultra-low power range of just 0.1 to 10 milliwatts, depending on the workload. This level of efficiency enables continuous AI processing directly on the device – even when running on tiny batteries.

But power efficiency is only half the story. ECS-DoT can also process AI models with up to 13 million parameters – a measure of how complex the AI model can be. This processing capacity is enough for demanding real-world tasks such as:

- Real-time object detection and classification through a camera
- Path planning and control loops for autonomous drones
- Voice and gesture recognition in wearable devices

- Interpreting biomedical signals (like ECG or oxygen saturation) directly on diagnostic tools

In benchmark tests, ECS-DoT demonstrated 20 to 90 times greater energy efficiency than many commercial AI chips under the same conditions – including processors from Syntiant, Ambiq, and other NPUs. While many of these competitors focus on narrow, fixed-function tasks (for instance, recognizing a single voice command), ECS-DoT is fully programmable and scalable, able to adapt to a wide range of changing workloads – a critical advantage for versatile applications.

ECS-DoT is also thermally efficient: it can operate without active cooling such as fans. This makes it ideal for products like AR glasses, compact drones, or handheld surgical tools, where heat buildup cannot be tolerated.

In short: ECS-DoT stands out not just for its minimal energy consumption, but for the amount of real AI performance it delivers within that tiny power budget – making it a perfect fit for the next generation of smart, connected devices.

Commercial Readiness & Scalability

The current version of Nanoveu's ECS-DoT chip is sampling to OEM customers through developer kits. This chip, done in TSMC 22nm, is getting pull from OEMs, which can result in integration deals in early 2026.

By mid-2025, the next version of the ECS-DoT chip is entering the final phase of development, progressing steadily toward production readiness. The company has already completed RTL (Register Transfer Level) verification – confirming that the chip's functional design is correct – and is now advancing through the remaining stages:

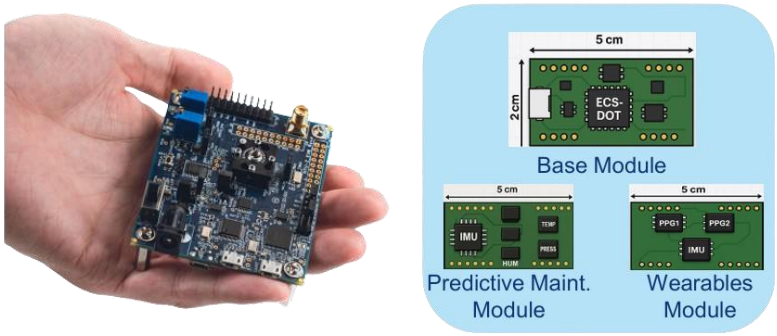
- Logic synthesis and power optimisation – translating design code into hardware logic while fine-tuning for ultra-low power consumption.
- Place-and-Route (P&R) with timing closure – physically mapping the circuits onto silicon to meet speed and timing targets.
- Pre-tape-out analysis – final power checks and design-rule reviews before fabrication.

These steps are ongoing and will culminate in the planned 16 nm tape-out at TSMC in Q4 2025.

The tape-out – the moment the finished chip design is sent for manufacturing – is scheduled for Q4 2025. It will run through a multi-project wafer (MPW) shuttle at TSMC's 16nm FinFET node – one of the most commercially relevant manufacturing processes for edge-AI chips. This process offers the right balance of performance, cost, and supply chain availability, ensuring ECS-DoT can be produced affordably and scaled quickly.

While ECS-DoT developer kits are already sampling to OEM customers, Nanoveu is gearing up to launch its next generation ECS-DoT modular developer kit in Q3 2025. These kits provide everything early customers need to experiment with the chip: evaluation boards, software development kits (SDKs), common interfaces like SPI, I^2C and UART, a library of pre-compiled AI models, and documentation to onboard engineering teams quickly. The goal is to let OEMs – whether they're drone makers, wearable brands, or med-tech developers – move from an idea to a working prototype in weeks instead of months.

Figure 2: Evaluation Board



Source: Nanoveu Investor Webinar, 9 July 2025, Slide 18.

ECS-DoT has also been designed with scalability in mind. Future versions can integrate more advanced memory, additional AI cores, or migrate to smaller process nodes (6nm or even 4nm) as manufacturing partnerships deepen and volumes grow. The modular architecture means Nanoveu can spin out application-specific chip variants – from high-volume consumer products like smartwatches to specialized industrial tools for drones or diagnostic equipment – without redesigning the entire chip from scratch.

From a commercial perspective, Nanoveu plans to turn early developer engagement into early chip sales starting in H1 2026. In the second half of 2026, Nanoveu expects to see ECS-DoT integrated into commercial devices, with early use cases emerging in autonomous drones, medical wearables, and predictive maintenance systems.

Use Case Deep Dive: Drone Applications

Why ECS-DoT matters for drones

Drones are one of the most promising use cases for edge AI, with demand spanning defense, logistics, infrastructure monitoring, and emergency response. But their biggest roadblocks are technical: limited battery power, strict weight limits, and the need to keep heat generation to a minimum. This is exactly where ECS-DoT changes the game.

Today, most drones either rely on cloud processing or small, inefficient CPUs. Both approaches have trade-offs: cloud-based AI requires constant data transmission and connectivity, while inefficient onboard processors drain batteries and shorten flight time. High-end modules like NVIDIA Jetson provide strong AI acceleration, but they consume so much energy that they're impractical for lightweight drones.

ECS-DoT fills this gap. The chip can perform complex AI computations directly onboard while drawing just 0.1 to 10 milliwatts of power. That means true autonomy is possible without compromising flight time or creating thermal problems – no bulky cooling systems required.

Simulations & flight testing with ECS-DoT

Nanoveu has already tested ECS-DoT in realistic drone scenarios. Using PX4 and Gazebo platforms, the chip handled key tasks like visual odometry, obstacle detection, and navigation. The results were striking: ECS-DoT maintained inference cycles of up to 50 hertz – more than three times faster than the 10–15 hertz typical for comparable embedded chips.

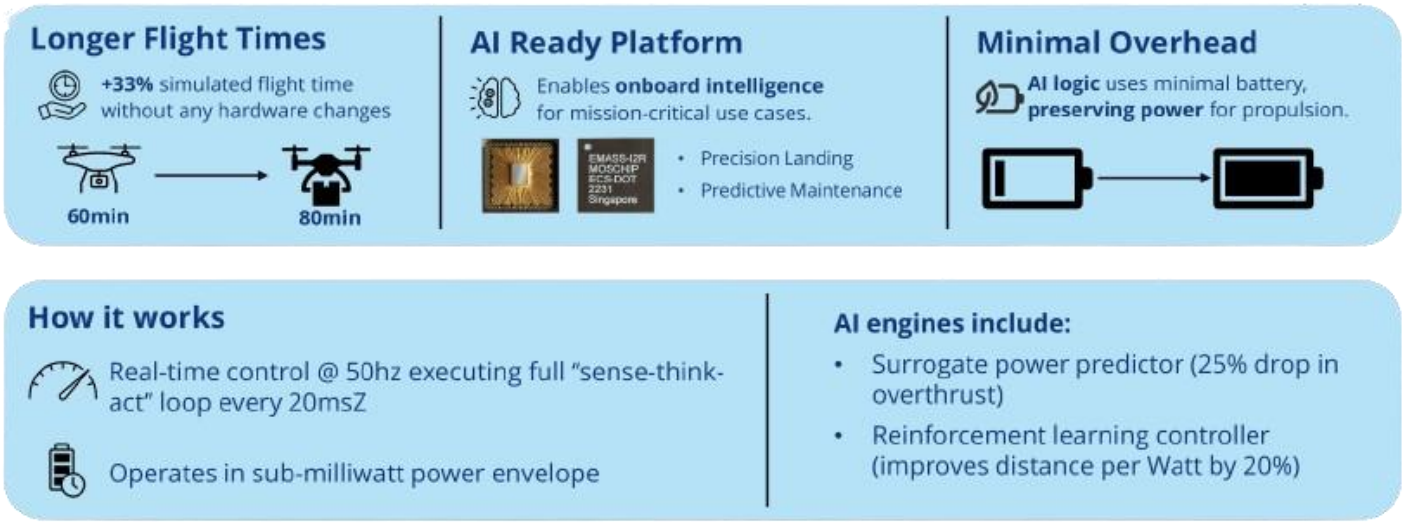
The chip's energy efficiency translated directly into performance gains. In simulation, drones using ECS-DoT achieved up to 33% longer flight times. Lower power draw means more energy stays available for the rotors, while removing bulky high-performance modules reduces weight and heat.

Phase-2 flight trials are now underway on both quadcopter and fixed-wing platforms. These tests are assessing real-world performance, thermal behavior, and integration stability – all critical data points for upcoming engagements with drone OEMs and system integrators.

What makes ECS-DoT so valuable for drones?

- Real-time response: ECS-DoT processes sensor data and issues control commands in microseconds – vital for flight stability, collision avoidance, and autonomous navigation.
- Extreme energy efficiency: Operating at just 0.1 to 10 milliwatts, ECS-DoT enables longer missions and higher payload efficiency without the need for active cooling.
- Onboard AI muscle: With capacity for AI models of up to 13 million parameters, ECS-DoT can run reinforcement learning, real-time image processing, and event-driven control loops directly on the drone – with no dependency on the cloud.

Figure 3: AI-Powered Efficiency for Drones



Source: Nanoveu Investor Webinar, 9 July 2025, Slide 20.

New possibilities unlocked by ECS-DoT

With ECS-DoT, drones can take on missions that were previously difficult or impossible:

- ISR missions (Intelligence, Surveillance, Reconnaissance): Drones can identify objects and plan routes locally, without needing a live network link.
- Logistics & delivery: Onboard AI enables smarter routing, obstacle avoidance, and adaptive control – even in urban or weather-challenged environments.
- Swarm AI: Multiple ECS-DoT-powered drones can share the workload, coordinating formations, navigating obstacles, and maintaining shared situational awareness – without relying on a central server.

Figure 4: Path to Market

Source: Nanoveu Investor Webinar, 9 July 2025, Slide 21.

What's next for commercial rollout?

These capabilities aren't just theoretical. ECS-DoT is already sampling to OEM customers and commercial engagements have started, with Nanoveu targeting both civil and defense drone manufacturers for the first wave of integrations.

Target Markets & Industry Themes

Edge AI (IoT, Wearables, Industrial)

The market for edge AI hardware, chips that run artificial intelligence directly on devices rather than in the cloud, is projected to reach USD 61.2 billion by 2030, reflecting a compound annual growth rate of 20.5 % according to IDC (2023). This growth is being driven by the rising need for real-time, low-latency processing in power-constrained devices that cannot depend on constant connectivity.

Demand is particularly strong in three areas. Wearables and health devices are forecast to reach USD 63.4 billion by 2025 (Statista, 2024) as smartwatches, fitness trackers and clinical diagnostic tools increasingly require on-device analytics rather than cloud reliance. Industrial IoT and automation is another major growth driver, expected to hit USD 106.1 billion by 2026 (MarketsandMarkets, 2023), as factories and infrastructure adopt predictive maintenance systems and smart sensors. Finally, autonomous drones and robotics are projected to be a USD 35.4 billion market by 2030 (Fortune Business Insights, 2023), with unmanned systems demanding local navigation, object recognition and decision-making. All of these markets share the same challenge: they require advanced AI capabilities delivered at very low power budgets. ECS-DoT's design is aimed directly at that gap.

Glasses-Free 3D & Spatial Interfaces

The global market for 3D displays and spatial interfaces is expected to grow from USD 17.7 billion in 2023 to USD 45.1 billion by 2030 (Allied Market Research, 2024), with demand accelerating as digital experiences evolve beyond flat screens. Consumer electronics manufacturers are exploring glasses-free 3D for gaming, video, and augmented reality on smartphones and tablets. Automotive companies are incorporating depth-aware head-up displays and dashboards, while the retail and digital signage industries are experimenting with immersive visuals to attract customer attention. EyeFly3D aligns with these long-term trends and offers a technological foundation that could become relevant as spatial computing and AR ecosystems continue to mature.

Smart Surface Coatings (Solar, Medical, Marine)

Smart coatings are a USD 3.6 billion industry today and are projected to grow to USD 8.0 billion by 2030 (MarketsandMarkets, 2024). These coatings provide functional benefits such as water repellency, dust and microbe resistance, and anti-corrosion properties. Their applications extend across several industries. In the solar sector, coatings keep photovoltaic and concentrated solar power surfaces cleaner for longer, improving efficiency and reducing maintenance costs. In marine and transportation settings, they protect against fouling and corrosion, extending the lifespan of valuable assets. In medical and hygiene contexts, antimicrobial coatings are becoming increasingly important for devices and surfaces that require a high standard of sterility. Nanoshield™ is already undergoing trials in several of these sectors, particularly in solar energy, where even a modest 3–6 % gain in energy yield or a 30–40 % reduction in cleaning cycles can have a meaningful economic impact for operators.

Competitive Landscape

Peer Group Overview

Nanoveu, through EMASS and its ECS-DoT chip, operates in the niche of Edge AI semiconductors. Only a small number of specialised companies are active in this space, each pursuing its own approach. Reviewing these peers helps to understand Nanoveu's positioning within the broader technology landscape.

Weebit Nano (ASX: WBT) is developing ReRAM (Resistive RAM), a next-generation non-volatile memory technology. ReRAM is designed to replace or complement conventional memory components by offering greater durability and lower power consumption. Weebit works with foundries and partners to integrate ReRAM into new chip designs, following a licensing-focused business model rather than manufacturing chips itself.

BrainChip Holdings (ASX: BRN) is focused on neuromorphic processors. These chips are modelled on the human brain and can recognise and process data such as images or sounds efficiently. BrainChip's "Akida" chip is designed to detect patterns in data directly on the device (at the "edge"), for example in automotive or security applications, without needing to send the data to the cloud.

Kinara is a US-based company that specialised in Edge AI chips for image and sensor data processing. Its chips were used in drones, cameras, and industrial applications. In early 2025, Kinara was acquired by NXP Semiconductors.

Ambiq Micro (NYSE: AMBQ) is a US company listed on the New York Stock Exchange since July 2025. Ambiq develops ultra-low-power chips based on its proprietary SPOT (Subthreshold Power Optimized Technology) platform. Its chips are used in a wide range of consumer and industrial products, including fitness trackers, smartwatches, medical wearables, and IoT sensors.

Syntiant is another US-based company, currently privately held. It focuses on always-on audio AI chips that can continuously listen without consuming much power. These chips enable functions such as voice commands ("Hey Siri," "Alexa") and sound recognition directly on the device. Syntiant's chips are already integrated into millions of headphones, speakers, and voice assistants.

Other reference players include Himax Technologies of Taiwan and Maxim Integrated (now part of Analog Devices). Himax produces image-processing ICs for cameras and AR glasses, while Maxim was long known for its ultra-low-power microcontrollers. While not directly comparable to Nanoveu, they illustrate the diversity of technologies and architectures across the wider Edge AI and low-power semiconductor ecosystem.

Benchmarking

Technical Benchmark

The following table (Table 1) compares five semiconductor devices designed for edge AI inference tasks, highlighting key differences in architecture, performance, power efficiency, and on-chip memory design. Although all five products aim to address the growing need for AI processing at the edge, they do so with distinct technical trade-offs and application focus.

Each column in Table 1 captures a core dimension of competitive differentiation in edge AI chips. Architecture defines the fundamental design choices, such as CPU core type and the presence of dedicated AI accelerators, that determine how well a chip can handle specific workloads. AI Performance, expressed in GOPS, measures raw computational capability, while AI Perf/Watt shows how efficiently that performance is delivered relative to power consumed. Power figures indicate energy draw in idle, typical, and peak states, a critical factor for battery-powered devices. On-Chip Memory reveals how much high-speed storage is embedded directly on the chip, reducing reliance on slower external memory and lowering latency. Finally, Package Size affects physical integration, with smaller formats offering greater flexibility for compact or weight-sensitive products such as drones, wearables, and embedded sensors.

Table 1: Technical Benchmark

Company / Chip	Architecture	AI Performance	AI Perf/Watt	Power	On-Chip Memory	Package Size
EMASS – ECS-DoT	Custom RISC-V core + 2x DL Accelerators	30 GOPS	3/15 TOPS	0.1 mW idle, 5 mW typical, up to 10 mW	2 MB SRAM + 2 MB MRAM (no DRAM)	5×5 mm QFN
Syntiant – NDP120	ARM Cortex-M0 + DSP + NN Core	6.4 GOPS	0.1/1 TOPS	0.25 mW idle, 9–27 mW typical, up to 30 mW	1 MB SRAM	5×5 mm QFN
Ambiq – Apollo4 Lite	ARM Cortex-M4F MCU (with DSP instr.)	0.24 GOPS	240/133 GOPS (MCU)	1 mW idle, 10–30 mW typical	1.8 MB SRAM + 2 MB MRAM	5×5 mm BGA
Himax	Proprietary vision MCU	0.8 GOPS	40/320 GOPS	2.5 mW idle, up to 20 mW	500 KB SRAM	n/a
Maxim Integrated	Mixed MCU/DSP	3.2 GOPS	1.6/64 GOPS	50 mW – 2 W	4 MB SRAM	n/a

Source: Company data, Nanoveu Webinar Presentation (July 2025), EMASS ECS-DoT Competitive Comparison (July 2025), Syntiant product brief, Ambiq MLPerf Tiny reports, Himax annual report (2024), Maxim Integrated product documentation. All performance, power, and memory values reflect typical edge AI inference configurations as disclosed by the respective companies or compiled by Nanoveu through internal benchmarking.

ECS-DoT, developed by EMASS, is built around a custom RISC-V architecture augmented by two dedicated deep learning accelerators. This combination enables the chip to reach up to 30 GOPS of AI compute performance, while maintaining ultra-low power consumption: just 0.1 mW in idle, 5 mW typical, and up to 10 mW peak. A major differentiator is its integrated memory: 2 MB of SRAM and 2 MB of MRAM, with no need for external DRAM. This not only improves energy efficiency but also reduces latency and board complexity. The chip is housed in a compact 5×5 mm QFN package.

Syntiant's NDP120 takes a more conventional architecture approach, combining an ARM Cortex-M0 processor with a DSP and a dedicated neural core. While its peak compute performance of 6.4 GOPS is lower than ECS-DoT, it is well suited for audio inference tasks such as wake-word detection or speech recognition. Power consumption is higher: 0.25 mW at idle, 9–27 mW typical, and up to 30 mW peak, and it includes 1 MB of SRAM. It uses the same 5×5 mm QFN footprint.

Ambiq's Apollo4 Lite is based on an ARM Cortex-M4F MCU without a dedicated AI accelerator, relying instead on software inference via Ambiq's SPOT technology. Its compute performance is significantly lower at 0.24 GOPS, but it compensates with

excellent power efficiency: 1 mW idle and 10–30 mW typical. The chip includes a combined 1.8 MB SRAM and 2 MB MRAM configuration and is packaged in a 5×5 mm BGA.

Himax offers a proprietary vision-focused MCU, with a peak performance of 0.8 GOPS and idle/active power consumption in the 2.5 mW to 20 mW range. While this chip is optimised for camera input and image processing tasks, its narrow use case and relatively modest 500 KB on-chip SRAM limit its flexibility. Package dimensions were not disclosed.

Maxim Integrated, now part of Analog Devices, delivers 3.2 GOPS using a mixed MCU/DSP architecture. However, its power consumption is significantly higher than the other chips in the comparison: between 50 mW and 2 W, putting it in a different thermal and system integration class. The chip does include a generous 4 MB of on-chip SRAM, but its design is oriented more toward general-purpose control or signal processing than lightweight AI workloads.

In summary, the architectural diversity across these chips reflects the fragmentation of edge AI use cases. Syntiant focuses on energy-efficient audio processing, Ambiq on ultra-low-power microcontrollers, Himax on image recognition, and Maxim on legacy control and DSP-heavy tasks. ECS-DoT, by contrast, is engineered as a general-purpose inference platform for multi-modal input—capable of handling audio, vision, and sensor fusion workloads simultaneously, while consuming single-digit milliwatts and requiring no external memory. This unique balance of compute performance, memory integration, and power efficiency positions ECS-DoT distinctly among edge inference solutions.

Task Benchmarks

The following table compares the real-world performance of three leading edge AI chips—ECS-DoT, Syntiant NDP120, and Ambiq Apollo4 Lite—across four standardised workloads: Visual Wake Words, Image Classification, Keyword Spotting, and Anomaly Detection. These results are derived from the 2025 MLCommons benchmarking framework and capture not only task execution speed (measured in milliseconds of latency) but also total energy consumption per inference (in microjoules). While datasheet specifications highlight theoretical peak performance, these benchmarks are far more relevant to developers and OEMs because they reflect actual application behaviour under low-power conditions.

Each row in Table 2 represents a specific AI workload commonly deployed in edge devices, with results shown for both latency (how quickly the task is completed) and energy consumption (how much power is used per inference). Visual Wake Words tests a chip's ability to detect visual triggers such as gestures or object presence, requiring fast reaction times and minimal energy for always-on operation. Image Classification measures how efficiently the chip can recognise and categorise still images, a proxy for vision-based AI tasks in drones, wearables, or cameras. Keyword Spotting evaluates continuous audio monitoring for wake phrases, balancing responsiveness with battery life. Anomaly Detection focuses on identifying irregular patterns in sensor data, a critical function for predictive maintenance, medical monitoring, and safety systems. Together, latency and energy results provide a holistic view of a chip's suitability for battery-powered, always-on AI applications, where both speed and efficiency are non-negotiable.

Table 2: Task Benchmark

Task	Metric	ECS-DoT	Syntiant NDP120	Ambiq Apollo4 Lite
Visual Wake Words	Latency (ms)	4.2	12.7	n/a
Visual Wake Words	Energy (µJ)	3.7	71.7	n/a
Image Classification	Latency (ms)	6.2	16	70–160
Image Classification	Energy (µJ)	5.5	101.8	~2,100
Keyword Spotting	Latency (ms)	3.9	4.4	22–54
Keyword Spotting	Energy (µJ)	3.1	31.5	~360
Anomaly Detection	Latency (ms)	1.2	n/a	2.3–5.7
Anomaly Detection	Energy (µJ)	0.8	n/a	~150

Source: MLCommons Inference Benchmarks (2025), Nanoveu internal testing and analysis (July 2025), Ambiq MLPerf Tiny (v0.7), Syntiant NDP120 datasheet. All latency and energy results refer to representative inference runs under low-power edge AI conditions. ECS-DoT results reflect internal testing by EMASS using the MLCommons reference workloads for visual, audio, and sensor classification tasks.

ECS-DoT consistently delivers best-in-class results across all four tasks, demonstrating not only high compute throughput but also extremely low energy requirements—making it uniquely suited for battery-constrained, always-on applications.

In the Visual Wake Words task, used to detect visual cues such as gestures or object presence that trigger device activity, ECS-DoT completes the inference in just 4.2 milliseconds, consuming a mere 3.7 microjoules. By contrast, Syntiant requires 12.7 ms and burns 71.7 µJ, while Ambiq provides no benchmark result here, as Apollo4 Lite is not equipped for vision-based AI tasks.

In Image Classification, which measures how quickly and efficiently a device can identify objects in still images, ECS-DoT completes the task in 6.2 ms, using only 5.5 µJ of energy. Syntiant is nearly three times slower at 16 ms and consumes over 101.8 µJ. Ambiq, not optimised for AI acceleration, performs poorly here: latencies range between 70–160 ms, with energy usage approaching 2,100 µJ per inference—nearly 400× more than ECS-DoT.

The results are equally decisive in Keyword Spotting, a core task for audio-first devices such as voice assistants. ECS-DoT recognises spoken triggers like “Hey Google” in 3.9 ms and just 3.1 µJ. Syntiant, despite its audio specialisation, is marginally slower at 4.4 ms and significantly less efficient, requiring 31.5 µJ, roughly 10× more energy. Ambiq once again trails, with 22–54 ms of latency and energy use near 360 µJ, a disparity of over 100× compared to ECS-DoT.

The final workload, Anomaly Detection, assesses how well a chip can detect irregular patterns in time-series sensor data, a key capability for wearables, medical devices, or industrial equipment. ECS-DoT performs the task in 1.2 ms, consuming only 0.8 µJ, while Ambiq completes the task in 2.3–5.7 ms but requires 150 µJ of energy. No benchmark data is available for Syntiant on this task, as it was not designed to support this modality.

Taken together, the MLCommons benchmarks confirm that ECS-DoT not only delivers industry-leading latency, but does so with an order-of-magnitude better energy efficiency than its closest competitors. Syntiant performs adequately in audio workloads but falls short in vision and classification tasks, while Ambiq excels as an ultra-low-power MCU but struggles with any AI use case requiring more than lightweight processing. ECS-DoT’s ability to handle multi-modal workloads, audio, vision, and anomaly detection, on a single chip, with single-digit milliwatt power profiles and sub-10 µJ inference costs, makes it a strong candidate for next-generation “always-on” edge devices such as XR headsets, drones, wearables, and sensor hubs.

Strategic Benchmarks

The competitive strategies across the edge AI and ultra-low-power chip ecosystem vary widely, reflecting each company's technological focus, monetisation path, and degree of commercial maturity.

Table 3: Strategic Benchmark

Company	Main Applications	Business Model	Development Stage
Nanoveu / EMASS	Audio, vision, sensor fusion, IoT, XR, wearables	Chip design; licensing potential	Dev kits launched; 22nm chip sampling; 16nm tape-out 2025; OEM tests ongoing
Weebit Nano	ReRAM memory IP	IP licensing	IP licensed to foundry partners
BrainChip	Neuromorphic vision & pattern recognition	Chips + licensing	Early pilots with OEMs
Kinara	Vision AI inference chips	Chip sales	Acquired by NXP (2025)
Ambiq	Wearables, IoT	Chip sales (MCU focus)	Commercial; IPO filed July 2025
Syntiant	Audio AI (wake word, speech)	Chip sales	Millions of chips shipped
Himax	Imaging for AR/camera	Chip/module sales	Established OEM base
Maxim Integrated	Ultra-low-power MCUs	Chip sales	Part of Analog Devices

Source: Company announcements, investor presentations, ASX filings (Nanoveu, Weebit Nano, BrainChip), acquisition disclosures (Kinara/NXP), IPO documentation (Ambiq), product briefs (Syntiant, Himax, Maxim Integrated), and Nanoveu peer benchmarking analysis (July 2025). All stage-of-development and business model insights reflect publicly available information as of August 2025.

Nanoveu, through its EMASS joint venture, remains at an early but rapidly advancing stage of its commercial journey. In 2025, the company launched developer kits built around its current ECS-DoT chip, enabling OEMs to evaluate real-world use cases in drones, wearables, and XR systems. Tape-out of the chip's next iteration—targeting TSMC's 16 nm node, is scheduled for late 2025, with physical silicon expected in 2026. Although Nanoveu currently follows a chip design and direct sales approach, it has publicly stated that future licensing remains an open avenue. This hybrid model could allow for capital-efficient scaling: combining near-term margin from chip deployments with longer-term IP licensing revenues across verticals.

Weebit Nano is positioned as a pure IP licensing company, focused on commercialising its ReRAM (Resistive RAM) technology. Rather than producing chips itself, Weebit licenses its memory IP to foundry and design partners, who integrate it into broader semiconductor products. This model avoids the capital intensity of manufacturing and provides scalable revenue potential, assuming successful technology adoption and recurring licence fees.

BrainChip occupies a unique niche with its Akida neuromorphic processor, inspired by the human brain's event-based architecture. It targets vision and pattern recognition tasks, and its go-to-market strategy centres around pilot engagements with OEMs. The company follows a blended model of chip sales and IP licensing, though at this stage, widespread commercial adoption remains limited to a handful of partners.

Kinara, a former specialist in vision inference silicon, was acquired by NXP in 2025, an indicator that global chip leaders are actively consolidating capabilities in edge AI through acquisition rather than in-house development. Kinara's exit underscores the strategic value of specialised architectures when matched with scale and distribution.

Ambiq, by contrast, is already fully commercial. Its ultra-low-power MCUs are widely deployed in wearables and IoT devices, and the company filed for an NYSE listing in July 2025. With a straightforward chip sales model and proven traction in volume markets, Ambiq represents a benchmark for translating energy efficiency into real-world market penetration.

Syntiant has also achieved significant commercial success, albeit in a more focused vertical: audio AI. Its edge chips power always-on voice triggers in millions of smart devices, from earbuds to home assistants. Its high-volume chip sales strategy leverages standardised form factors and tight application targeting to drive adoption in embedded systems.

Himax and Maxim Integrated (now part of Analog Devices) represent mature, well-established incumbents in adjacent fields. Himax has built a strong position in camera and AR imaging silicon, while Maxim has long been a trusted supplier of ultra-low-power mixed-signal MCUs for industrial and medical use cases. These companies operate with deeply entrenched OEM relationships and mature revenue bases, but have limited exposure to AI-specific workloads or edge inference acceleration.

Taken together, the strategic positioning of these players reflects a highly segmented market. Weebit Nano and BrainChip represent IP-first models with long-term optionality but shorter-term revenue unpredictability. Ambiq and Syntiant prioritise high-volume chip sales in tightly defined application domains. Kinara has exited via acquisition, and Himax and Maxim continue as established suppliers. In this context, Nanoveu occupies a unique hybrid role: a young chip company with a flexible model that bridges between direct silicon sales and potential IP licensing, and a platform architecture that supports multi-modal AI workloads, audio, vision, and sensor fusion—on a single low-power chip.

This blend of architectural breadth and strategic optionality offers Nanoveu several pathways to scale: as a full-stack chip vendor, a licensing partner for specific domains (e.g., XR or IoT), or a platform player enabling OEMs to consolidate multiple AI functions into a single compact footprint. As OEM testing continues and ECS-DoT progresses toward silicon tape-out, Nanoveu's trajectory will hinge not just on performance—but on how it chooses to monetise the edge.

Financial Comparison

A detailed financial comparison of Nanoveu (ASX: NVU) and its listed peers in the semiconductor and edge AI ecosystem reveals substantial differences in commercial maturity, capital structure, revenue profile, and market valuation logic. Despite being at a pre-revenue stage, Nanoveu is already assigned a market value that implies considerable investor confidence in the potential of its ECS-DoT chip platform. The company's valuation must be viewed not through the lens of historical earnings, but rather through the optionality embedded in its intellectual property, the capital-light execution model, and the strategic leverage associated with successful developer kit adoption and OEM design wins.

In FY2024, Nanoveu reported total revenue of just A$0.007 million, with no contribution yet from ECS-DoT. This places the company at the earliest stage of commercialisation among its listed peers. BrainChip, while facing executional challenges of its own, generated A$1.0 million, mainly through early chip shipments. Weebit Nano posted A$1.0 million in IP licensing income, demonstrating first signs of monetisation through foundry partnerships. At the other end of the spectrum, Himax Technologies delivered A$1,406.0 million in revenue from mature commercial products, while CEVA and Lattice Semiconductor generated A$166.0 million and A$790.0 million respectively, underpinned by scalable IP and chip portfolios.

R&D intensity is another point of divergence. Nanoveu reported A$0.00 million in research and development costs in FY2024, significantly below its peers. Weebit and BrainChip invested A$13.0 million and A$8.0 million respectively, while Himax, CEVA, and Lattice reported A$249.0 million, A$111.0 million, and A$247.0 million. Nanoveu's comparatively low expenditure is not necessarily a weakness: most ECS-DoT development is conducted through EMASS and capitalised off balance sheet. While this suppresses reported R&D figures, it also reduces cash burn and avoids dilution, an

advantage if execution remains on track. However, it does mean investors must look beyond financial statements to assess true technical progress.

Nanoveu's P/B ratio of 23.2x, based on A$3.2 million in equity post-capital raise, is high relative to commercial peers such as Himax (1.5x) and CEVA (2.0x), but in line with BrainChip (21.5x) and above Weebit (5.4x). The valuation gap underscores market perception that Nanoveu's current book value understates its intellectual property pipeline. In IP-centric models, high P/B ratios are often indicative of unrecognised architecture value or pre-commercial licensing potential, though they also expose companies to sentiment-driven volatility if technical delivery falls short.

Crucially, Nanoveu operates with a clean capital structure. Following the repayment of its only short-term loan, the company holds no financial debt. It concluded a A$3.0 million capital raise in July 2025, bringing its cash balance to approximately A$4.5 million. This positions Nanoveu as one of the most conservatively structured companies in its peer group, though its short runway implies near-term reliance on either revenue traction or further capital raises. In contrast, Weebit and BrainChip have more comfortable cash positions, A$88.0 million and A$21.0 million respectively but also run significantly larger cost bases. Nanoveu's ability to preserve capital while advancing product development gives it flexibility but also compresses its execution window.

In summary, Nanoveu presents a highly asymmetrical investment case. It lacks historical revenue, it lacks visibility on OEM adoption, and its valuation appears inflated by conventional metrics. Yet when compared to early-stage peers, Nanoveu is not overvalued, it is valued in anticipation. Investors are not buying discounted cash flow, they are buying the potential for ECS-DoT to unlock licensing or product revenue across multiple verticals. The upside case hinges on the successful validation of the chip's architecture, followed by conversion into revenue-bearing engagements. The downside risk is not zero—but is partially mitigated by the company's debt-free balance sheet, lean cost model, and focused development roadmap.

If ECS-DoT delivers on its promise, whether through performance benchmarks, developer kit traction, or early OEM pilots, Nanoveu's current valuation may prove conservative. If it does not, the company's short cash runway will likely require further dilution. Either way, Nanoveu is no longer simply a technology narrative—it is a binary commercialisation thesis now entering its critical test phase.

Table 4: Financial Comparison

Company	Market Cap (in M)	Enterprise Value (in M)	FY24 Revenue (in M)	COGS (in M)	Gross Margin %	EBITDA (in M)	EBITDA Margin	R&D (in M)	R&D % of Revenue	EV/Sales	P/B	Cash (in M)
ASX-Listed Peers												
NANOVEU LIMITED (XASX:NVU)	$74	$68	$0	$0	47%	-$3	-39869%	$0	-774%	10410	23.2	$5
WEEBIT NANO LTD (XASX:WBT)	$519	$431	$1	n/a	n/a	-$49	-3652%	-$13	-965%	318	5.4	$88
BRAINCHIP HOLDINGS LTD (XASX:BRN)	$425	$405	$1	$1	14%	-$23	-3793%	-$8	-1248%	656	21.5	$21
US-Listed Peers												
Himax Technologies, Inc. (XNAS:HIMX)	$1,971	$2,456	$1,406	$977	30%	$140	10%	$249	18%	1.7	1.5	$338
LATTICE SEMICONDUCTOR CORPORATION (XNAS:LSCC)	$13,052	$12,854	$790	$262	67%	$53	7%	$247	31%	16.3	11.8	$198
QUICKLOGIC CORPORATION (XNAS:QUIK)	$145	$117	$31	$18	41%	$0	1%	$8	25%	3.8	3.5	$27
CEVA, INC (XNAS:CEVA)	$805	$776	$166	$20	88%	-$5	-3%	$111	67%	4.7	2.0	$29
NXP Semiconductors NV (XNAS:NXPI)	$80,953	$77,297	$19,552	$8,516	56%	$5,543	28%	$888	5%	4.0	3.9	$4,431
MICROCHIP TECHNOLOGY INCORPORATED (XNAS:MCHP)	$51,754	$127,064	$68,225	$29,972	56%	$1,046	2%	$888	1%	1.9	33.6	$11,961

Source: Company filings (ASX and SEC), trailing twelve-month (TTM) financial data derived from FY2024 and CY2025 reports, investor presentations, and Bloomberg data as of 9 August 2025. All figures are converted to Australian dollars (AUD) using an exchange rate of USD 1 = AUD 1.55. Differences in reporting currencies, fiscal year ends, and disclosure formats have been normalised to enable meaningful comparison across the peer group.

Commercial Roadmap

Tape-Out Timeline & Dev Kit Launch

Nanoveu has already completed initial fabrication runs of the ECS-DoT chip, with functional silicon successfully tested across multiple applications. These first-generation chips have demonstrated their capabilities in internal benchmarks, drone simulations, and hardware-in-the-loop evaluations, meeting the company's performance and power efficiency targets. Based on our discussions with management, the current version is already integrated into working evaluation boards and is shipping to selected partners via the ECS-DoT Developer Kit.

The next tape-out, scheduled for Q4 2025, marks a key inflection point in the commercialisation roadmap. This version of ECS-DoT, fabricated on TSMC's 16nm FinFET process, introduces architectural refinements aimed at further reducing power consumption, optimising die area, and expanding AI model compatibility. The chip will be produced via a multi-project wafer (MPW) shuttle, allowing Nanoveu to secure updated silicon quickly and cost-effectively before committing to larger production lots.

A new Modular Developer Kit, available from Q3 2025, includes the functional ECS-DoT chip, evaluation boards, precompiled AI models, and development tools. It supports standard interfaces such as I^2C, SPI, and UART, and is designed to give OEM partners a seamless pathway from prototyping to integration. This staged rollout strategy significantly shortens the time from first technical engagement to potential design-in.

Partner Engagement & Go-to-Market Path

Nanoveu's go-to-market strategy revolves around early OEM engagement. Instead of building the chip and hoping the market comes, Nanoveu is already engaging with drone makers, wearable brands, and industrial integrators who need exactly what ECS-DoT offers.

The plan is straightforward: Developer Kits go out to select partners, giving them the tools to evaluate ECS-DoT in their own systems and start application development. From there, those evaluations are expected to lead early chip sales to validate the ECS-DoT in a physical design. These early chip sales are the bridge to design-ins – the point where ECS-DoT becomes a built-in part of an OEM's future product roadmap.

Commercial Milestones Expected 2025–2026

The next 18 months will be pivotal for Nanoveu. First Developer Kits are shipping to selected partners, kicking off the hands-on testing phase. The tape-out in Q4 2025 will produce the next generation of ECS-DoT chips, with initial silicon samples expected shortly after.

Nanoveu aims for early chip sales in H1 2026, formalising the partnerships that will bring ECS-DoT into real products. In H2 2026, the company expects to see initial product integrations – drones, medical wearables, and industrial devices that start to use ECS-DoT not as a test platform, but as a key component.

Financials & Capital Structure

Historical Financials Snapshot

Nanoveu has undergone a fundamental transformation over the past two years, evolving from a niche player in advanced display and surface coating technologies into a high-conviction semiconductor company focused on ultra-low-power Edge AI processing. The turning point came with the acquisition of EMASS in October 2024 – a specialist SoC developer targeting battery-constrained smart devices, autonomous systems, and IoT infrastructure.

Revenue from Nanoveu's legacy products (EyeFly3D™, Nanoshield™) remained modest, with FY24 revenue totalling A$514k, down ~15% YoY (FY23: A$605k). The Group reported a net loss of A$4.2 million, reflecting heightened R&D investment tied to ECS-DoT chip development, IP protection, and expanded engineering operations.

As of H1 FY25 (31 Dec 2024), Nanoveu recorded a net operating cash outflow of approximately A$2.1 million. The balance sheet remains clean, with A$4.5 million in cash, minimal liabilities (A$0.8 million), and no interest-bearing debt.

From a technology standpoint, Nanoveu has now moved beyond pure R&D into early-stage commercialisation. Its first-generation 22nm ECS-DoT chip has been completed and is currently deployed in evaluation kits with global OEMs in the wearables and drone sectors. The chip is supported by a full software development kit (SDK), and early feedback suggests that EMASS is on track to secure initial design wins and transition to production volumes.

Meanwhile, development of the next-generation 16nm ECS-DoT is well underway. Tape-out via a TSMC Multi-Project Wafer (MPW) shuttle is on track for Q4 CY2025, with engineering led by a 24-member international team in collaboration with the Center for Nanoelectronics and Devices (CND). This version will support enhanced power/performance characteristics and adopt compact BGA packaging for embedded deployment.

While historical financials still reflect Nanoveu's legacy profile, the company is now technically and organisationally positioned to unlock commercial revenue in 2026 and beyond. The transition from a loss-making IP incubator to a hardware-driven AI business is in motion – and the financial inflection point is expected to follow.

Capital Raisings, Options, Performance Rights

Nanoveu has strategically utilised equity markets and option-based instruments to fund its transition into semiconductor commercialisation, while maintaining a clean and debt-free capital structure. Over the course of FY25, the company secured A$6.22 million

in gross proceeds through a combination of placements and an underwritten option facility.

In May 2025, Nanoveu raised A$3.02 million via the issue of 97.5 million shares at $0.031, accompanied by one-for-two free attaching options (NVUO, ex. $0.045). This was followed by a second placement in July 2025, raising A$2.70 million through 49 million shares at $0.055, with one-for-four attaching options (NVUO, ex. $0.08).

To further support short-term funding, Nanoveu also entered into an option underwriting agreement in June 2025, covering 12.5 million NVUO options at an exercise price of $0.04. This agreement provided an additional A$500,000 in committed capital, bringing total gross funding in FY25 to A$6.22 million.

Beyond these direct capital raisings, Nanoveu has structured a multi-year pathway for additional cash inflows through staged option exercises. Based on management assumptions, over 248 million options are forecast to be exercised between FY25 and FY30, generating an estimated A$8.3 million in future proceeds. The bulk of these inflows is expected between FY26 and FY28, aligning with Nanoveu's commercial ramp-up.

In parallel, the company has deployed equity-based incentives via performance rights (PRs) to attract and retain top engineering and commercial talent. Over 130 million PRs have been granted to date, with vesting subject to strict share price hurdles and operational milestones. The largest tranches are expected to convert between FY26 and FY28, in line with expected design wins and commercial deployment of the ECS-DoT chip.

While this combination of options and PRs results in a projected increase in shares on issue from ~919 million (FY25 start) to ~1.34 billion (FY30), Nanoveu's capital strategy ensures that dilution is directly linked to performance outcomes and accompanied by balance sheet strengthening. The company continues to avoid debt financing and retains flexibility to scale without balance sheet overhang.

Based on recent funding and modelled option inflows, Nanoveu is forecast to be funded through to late CY25 under a base case scenario. This covers the ECS-DoT tape-out at TSMC, early silicon fabrication, Dev Kit distribution and initial revenue generation. Should further working capital be required for volume production or customer onboarding, the company retains ample headroom for follow-on equity issuance without materially exceeding historical dilution levels.

Finally, Nanoveu's funding strategy is disciplined, performance-aligned and growth-focused. The combination of strategic placements, structured option liquidity and milestone-based equity incentives provides the necessary financial runway to scale into Edge AI commercialisation without compromising control or capital integrity.

Valuation

Nanoveu's valuation is based on a detailed bottom-up Discounted Cash Flow (DCF) model that reflects the expected scale-up of its ECS-DoT chip business through to calendar year 2035 (CY35). The model incorporates all major revenue streams – including pre-production sales generated during customer validation stages (Engineering, Design, and Production Validation Testing), volume chip sales following design-in conversion, and residual contributions from the legacy Nanoshield and EyeFly3D products. Based on these assumptions, the model indicates an implied target price of **A$0.26** per share.

Revenue Assumptions and Growth Trajectory

The The financial forecast for Nanoveu is structured from the ground up, mapping the company's step-by-step route from initial customer engagement to high-volume ECS-DoT chip shipments, while also factoring in the steady but diminishing revenue contribution from Nanoshield and EyeFly3D. The model follows the company's

commercialisation logic: early technical evaluation through Developer Kits, conversion of a portion of these engagements into confirmed design wins, and a structured ramp through industry-standard validation phases before mass production.

Developer Kits are the first point of entry, allowing OEMs and system integrators to evaluate ECS-DoT in their own hardware environments and begin software integration. Shipments are projected to grow from just three kits in CY25 to over 1,600 by CY36. The model assumes a gradually rising conversion rate — starting at 30% in CY25–CY26, increasing incrementally to 35% by CY34–CY35, before easing back to 30% in CY36. This trajectory reflects the expectation of higher conversion efficiency as market adoption accelerates and Nanoveu's platform matures, followed by a slight moderation in later years as the company penetrates more challenging customer segments.

Once a design win is secured, the project progresses through three key pre-production stages: Engineering Validation Test (EVT), Design Validation Test (DVT) and Production Validation Test (PVT). In the base case, EVT involves approximately 100 units at a price of A$20 per unit (A$2,000 total), DVT around 500 units at the same price (A$10,000 total), and PVT about 2,000 units at A$20 each (A$40,000 total). Together, these phases generate roughly A$52,000 per deal in pre-production revenue in CY25, with this figure indexed annually for inflation in the model. These sales occur before mass production begins, providing early cash flow and strengthening customer commitment.

Mass production volumes per design win are set at 90,000 units in the early years (Conversion Chip Rate of 55%), increasing to 120,000 units from CY29 and up to 150,000 units in later-stage projects (Conversion Chip Rate up to 58%). This variation reflects different verticals — lower volumes in drones, higher volumes in robotics and industrial edge devices, and even larger potential in future applications. Average selling prices start at A$7.60 in CY25 and gradually rise to A$9.30 by CY35, factoring in modest inflation and a strengthening value proposition. Based on an expected cost of goods sold of A$3.00–3.20 per chip, the model supports a 60% gross margin target. As early design wins enter mass production, chip sales ramp sharply from CY27 and are forecast to exceed A$511 million by CY35.

Alongside ECS-DoT, Nanoshield revenues are modelled from a growing client base, each generating approximately A$100,000 annually (indexed with inflation), while EyeFly3D maintains an ARPU starting at A$75,000 with annual inflation adjustments. These product lines provide stable, lower-risk cash flow in the short term, but their share of total revenue declines as ECS-DoT scales.

By design, the model anticipates a revenue mix transition: in the initial three years, Developer Kits, pre-production shipments, and legacy products dominate, but from CY28 onwards, mass-production chip sales become the main driver. This shift accelerates in the early 2030s, creating a steep, high-leverage growth trajectory consistent with successful semiconductor commercialisation cycles.

Table 5: Revenue Assumptions

Revenue Assumptions	CY25	CY26	CY27	CY28	CY29	CY30	CY31	CY32	CY33	CY34	CY35
ECS-DoT Chip											
DevKits	3	9	23	63	177	354	601	962	1,299	1,507	1,628
Conversion Rate	30%	30%	31%	32%	32%	33%	33%	34%	34%	35%	35%
Deals	1	3	7	20	57	117	198	327	442	527	570
Pre Production Revenue per Deal	52,000	53,040	54,101	55,183	56,286	57,412	58,560	59,732	60,926	62,145	63,388
Pre Production Revenue	**0.05**	**0.14**	**0.39**	**1.12**	**3.19**	**6.70**	**11.62**	**19.54**	**26.91**	**32.78**	**36.11**
Conversion Chip Rate	55%	55%	56%	56%	57%	57%	58%	58%	58%	58%	58%
Chip Volume	90,000	270,000	725,400	2,021,760	6,793,114	14,010,797	29,772,943	49,080,246	66,258,332	79,120,243	85,449,863
ASP	7.6	7.8	7.9	8.1	8.2	8.4	8.6	8.7	8.9	9.1	9.3
Chip Sales	**0.38**	**1.15**	**3.21**	**9.13**	**31.85**	**67.01**	**147.80**	**248.51**	**342.20**	**416.80**	**459.15**
Nanoshield	**0.30**	**0.51**	**0.78**	**1.19**	**1.83**	**2.79**	**3.99**	**5.70**	**7.56**	**9.25**	**10.38**
Client	3	5	8	11	17	25	35	50	64	77	85
ARPU	100,000	102,000	104,040	106,121	108,243	110,408	112,616	114,869	117,166	119,509	121,899
EyeFly3D	**0.23**	**0.38**	**0.59**	**0.90**	**1.37**	**2.10**	**2.57**	**3.14**	**3.84**	**4.70**	**5.76**
Client	3	5	8	11	17	25	30	36	44	52	63
ARPU	75,000	76,500	78,030	79,591	81,182	82,806	84,462	86,151	87,874	89,632	91,425
Total Revenue	**0.95**	**2.19**	**4.97**	**12.34**	**38.24**	**78.61**	**165.98**	**276.90**	**380.52**	**463.54**	**511.40**

Cost Structure, Operating Leverage and Margin Expansion

Cost of Sales is expected to normalise quickly after an initial anomaly of –75% in CY25, reflecting one-off accounting impacts in the transition year. From CY26 onwards, CoS improves gradually from 42% to 37% by CY33, where it stabilises through the remainder of the forecast period. This trend reflects economies of scale, supply chain efficiencies, and a higher proportion of high-margin ECS-DoT chip sales in the revenue mix.

Operating expenses (OPEX) are elevated in the initial years of commercialisation, as Nanoveu invests heavily in R&D, customer acquisition, and market entry. As revenues scale and these fixed investments are leveraged across a broader base, OPEX gradually declines as a percentage of revenue, reaching around 32% by CY30.

This cost discipline, combined with stable gross margins, drives a steady improvement in profitability. EBITDA margins shift from negative during the early ramp-up years to 30% by CY30.

Capital Expenditure and Free Cash Flow

Capital expenditure remains modest over the forecast horizon and is primarily allocated to software development and intellectual property (IP) assets. This reflects Nanoveu's fabless business model, where capital intensity is far lower than in traditional semiconductor manufacturing. CapEx is focused on supporting continuous product innovation, software upgrades, and the protection of proprietary design elements, ensuring the ECS-DoT platform remains competitive as the market evolves.

In the first three forecast years (through CY27), payments for intangible assets are modelled as fixed at approximately A$2.8 million annually, indexed for inflation. From CY28 onwards, these payments are tied directly to revenue performance – initially set at around 25% of revenue and declining progressively to 8% by the end of the forecast period. This phased approach reflects the front-loaded investment required to establish Nanoveu's IP base and the lower ongoing maintenance cost as the core technology platform matures.

This lean capital allocation strategy allows Nanoveu to scale without the heavy infrastructure burden typical of chip manufacturers, supporting stronger free cash flow generation and improving capital efficiency metrics as the business transitions from product introduction to sustained growth.

Working Capital Assumptions

The model reflects working capital dynamics aligned with Nanoveu's current balance sheet structure. Trade and other receivables remain minimal in the early years (A$0.14m in CY25e), representing short average collection periods of around 30–40 days during the pre-commercial phase. Payables are projected to expand in line with production ramp-up, increasing from A$0.56m in CY25e to A$17.39m by CY30e, reflecting extended supplier terms of approximately 45–60 days with foundry and component partners. Inventory holdings are not separately recorded, consistent with the company's fabless model, where production is outsourced and physical stock exposure is limited.

As ECS-DoT shipments scale, both receivables and payables grow proportionally, but the net working capital requirement remains modest relative to revenue. This is due to the combination of short receivables cycles, supplier credit, and minimal inventory. The largest working capital expansion is expected between CY27e and CY29e as OEM orders move to volume production. Thereafter, improved cash conversion from established customers helps stabilise the working capital profile, supporting free cash flow generation without significant additional funding requirements.

The company's only short-term borrowing of A$0.12m (recorded in CY24) was fully repaid in January 2025, leaving Nanoveu debt-free ahead of its commercial scale-up phase. In addition, a loan receivable of A$0.26m recorded in CY24 is expected to be fully repaid by no later than CY26, further strengthening the company's cash position.

Capital Structure and Cost of Capital Assumptions (WACC)

The model uses a Weighted Average Cost of Capital (WACC) of 14.99% to discount future cash flows. The applied beta of 1.95 is based on a 1-year regression against the ASX Small Ordinaries Index, reflecting the typical risk profile of Australian tech small caps. Other inputs include a risk-free rate of 4.30%, a cost of equity of 15%, and a pre-tax cost of debt of 12%. The capital structure assumes a moderate level of gearing.

To support growth funding requirements, the model incorporates two equity raisings: A$5 million in CY25 at an issue price of A$0.10 and a further A$9 million in CY26 at A$0.14. These raisings are included in the fully diluted share count and ensure adequate working capital during the commercial scale-up phase.

On this basis, total ordinary shares on issue are projected at 1,418.08 million on a fully diluted basis. This figure reflects the current issued capital, the impact of all in-the-money options at their respective exercise prices, and the forecast equity raisings embedded in the model. No additional convertible securities or other dilutive instruments are assumed beyond these, ensuring alignment between the fully diluted share count and the projected capital structure over the forecast horizon.

Terminal Value Approach and Valuation Outcome

The valuation is anchored in a terminal growth methodology, applying a long-term growth rate of 3.5%. This results in a terminal value of A$1,175 million. The sum of the discounted terminal value (A$246 million) and the discounted forecast cash flows yields an enterprise value of A$171 million. After adjusting for the projected net cash position of A$192 million in CY35, the equity value comes to A$363 million. After accounting for all options, performance rights and future dilution events, the fully diluted share count reaches 1,418.08 million by the end of the model period, resulting in an implied target price of **A$0.26** per share.

Table 6: NVU Valuation

NVU Valuation (A$M)			
Terminal Growth Rate	3.5%	**WACC**	
Discount Rate	14.99%	Beta	1.95
Terminal Value (TV)	1,144.02	Rf	4.30%
Present Value of TV	246.13	Re	14%
Enterprise Value	**170.45**	Rd	12%
Net Debt	-192.08	E	61.66
Equity Value	**362.53**	D	0.33
Fully Diluted Shares	1,418.08	1-T	70%
Implied (Target) Price	**$0.2556**	**WACC**	**14.02%**

Sensitivity Analysis and Conclusion

The valuation output demonstrates relatively low sensitivity to moderate changes in key discounting assumptions. Across a realistic range of Weighted Average Cost of Capital (WACC) values (13.5% to 16.5%) and terminal growth rates (2.0% to 5.0%), the implied equity value per share fluctuates within a fairly narrow band – from A$0.2332 to A$0.2848.

The base case scenario (WACC of 15.0% and terminal growth of 3.5%) yields a valuation of **A$0.26** per share. Even under more conservative assumptions – for example, a higher WACC of 16.5% and terminal growth of 2.0% – the model still returns a value above A$0.2332 per share, indicating a strong degree of resilience in the valuation framework. Conversely, more optimistic assumptions lead to upside beyond A$0.2848 per share.

This stability underlines the robustness of the valuation, which is underpinned by recurring engineering revenues, operating leverage, and a capital-light scaling model. It suggests that Nanoveu's fair value is not unduly dependent on narrow parameter windows, providing greater confidence in the derived target price.

Table 7: Sensitivity Analysis

		WACC						
	25.56	13.5%	14.0%	14.5%	15.0%	15.5%	16.0%	16.5%
Terminal Growth	2.0%	23.36	23.35	23.34	23.34	23.33	23.33	23.32
	2.5%	24.04	24.03	24.03	24.02	24.01	24.01	24.00
	3.0%	24.78	24.77	24.77	24.76	24.75	24.75	24.74
	3.5%	25.58	25.58	25.57	**25.56**	25.56	25.55	25.55
	4.0%	26.46	26.45	26.45	26.44	26.44	26.43	26.42
	4.5%	27.42	27.42	27.41	27.40	27.40	27.39	27.39
	5.0%	28.48	28.47	28.47	28.46	28.45	28.45	28.44

Overall, the model presents a robust and conservatively constructed view of Nanoveu's long-term potential. It highlights how the company can create significant shareholder value through systematic commercialisation of its chip designs and strong operating leverage. While assumptions are intentionally cautious, the outcome points to an attractive risk/reward profile as Nanoveu transitions from engineering success to commercial scaling.

Risks & Execution Challenges

Execution Risk Post-Tape-Out

While the current ECS-DoT chip is silicon verified and can lead to commercial revenue, and the next generation design is complete and the company is preparing for tape-out via a multi-project wafer (MPW) shuttle at TSMC in Q4 CY25, manufacturing risk remains. Any delays or issues during the fabrication process – such as silicon bugs, yield

problems, or design-to-silicon mismatches – could affect time-to-market or require additional engineering cycles, potentially delaying revenue recognition.

Conversion Risk from DevKits to Volume Sales
The commercial model hinges on the successful conversion of Developer Kit recipients into OEM customers. While the model assumes a 30% conversion rate, the actual figure will depend on customer feedback, integration timelines, and competing solutions. If conversions fall materially short, revenue forecasts could miss their mark, delaying breakeven and weakening cash flow assumptions.

Competitive Pressure and Technological Substitution
The edge AI chip market is rapidly evolving, with strong competition from incumbents like Ambiq, Syntiant, and larger players such as Apple and Qualcomm. These companies possess deeper R&D resources, broader customer bases, and established ecosystems. Nanoveu's ability to differentiate its technology and secure design wins will be critical to gaining traction in such a competitive landscape.

Capital Requirements and Dilution Risk
While the company is forecast to hold a healthy net cash position, our model includes a A$5 million equity raise in CY26 to support scaling activities. If execution is slower than expected or if opex runs higher, additional capital may be required – increasing the risk of shareholder dilution.

Dependency on Strategic Partners and Supply Chain Fragility
As a fabless semiconductor company, Nanoveu relies on external foundries (TSMC) and packaging/test partners. Any disruptions in the global semiconductor supply chain – or geopolitical tensions involving Taiwan – could impact cost structures or delay product availability, especially at volume scale.

Ongoing Focus on Legacy Products
While Nanoshield and EyeFly3D still contribute to revenue, their strategic relevance is diminishing. There is a risk that continued support of these legacy products may divert management attention or resources from the company's high-growth core chip business. Their ability to scale profitably also remains uncertain.

Regulatory and IP Protection Risks
As Nanoveu expands globally, regulatory compliance will become more complex – particularly regarding export controls, device certification, and data security. Additionally, the protection of proprietary IP (especially in Asia) will be essential to sustaining any competitive advantage, particularly as the value lies heavily in software and algorithm design.

Appendix

Financials

Income Statement *A$'000s*	CY24	CY25e	CY26e	CY27e	CY28e	CY29e	CY30e
Revenue	0.01	0.95	2.19	4.97	12.34	38.24	78.61
Cost of sale of goods	0.00	-0.40	-0.90	-1.99	-4.81	-14.53	-29.87
Gross Profit	**0.01**	**0.55**	**1.29**	**2.98**	**7.53**	**23.71**	**48.74**
Operating expenses	-2.77	-2.26	-2.75	-4.18	-7.59	-14.95	-24.84
EBITDA	-2.74	-1.68	-1.43	-1.16	-0.01	8.82	23.97
D&A	-0.11	-0.95	-0.97	-0.99	-0.87	-0.96	-1.98
EBIT	-2.85	-2.63	-2.40	-2.15	-0.89	7.86	21.99
Net Interest	0.00	-0.00	-	-	-	-	-
NPBT	-2.85	-2.63	-2.40	-2.15	-0.89	7.86	21.99
Tax expense	-	-	-	-	-	-2.36	-6.60
NPAT	-2.85	-2.63	-2.40	-2.15	-0.89	5.50	15.39
Profit attributable to NCI	-2.85	-2.94	-2.60	-2.28	-0.92	5.60	15.60

Balance Sheet *A$'000s*	CY24	CY25e	CY26e	CY27e	CY28e	CY29e	CY30e
Cash	0.50	6.16	11.46	9.33	4.63	2.17	10.10
Trade and other receivables	0.50	0.14	0.35	0.60	1.23	3.82	7.86
Current assets	0.99	6.30	11.81	9.92	5.86	6.00	17.96
PPE	0.06	0.05	0.05	0.06	0.06	0.05	0.04
Right of use asset	0.01	0.05	0.04	0.03	0.02	0.01	0.01
Intangible Assets and Other	0.26	2.67	4.72	7.87	18.41	34.04	43.88
Non-current assets	0.33	2.77	4.81	7.95	18.48	34.10	43.93
Total assets	1.32	9.07	16.63	17.88	24.34	40.09	61.88
Trade and other payables	0.53	0.56	1.38	2.72	6.30	12.70	17.39
Borrowings	0.33	-	-	-	-	-	-
Other	0.33	0.34	0.41	0.61	1.84	4.23	6.97
Current liabilities	0.98	0.90	1.78	3.33	8.13	16.93	24.36
Borrowings	-	-	-	-	-	-	-
Other liability	-	0.11	1.08	3.30	7.15	14.89	23.55
Non current liabilities	-	0.11	1.08	3.30	7.15	14.89	23.55
Total Liabilities	0.98	1.01	2.86	6.63	15.29	31.82	47.91
Net Assets	0.34	8.06	13.76	11.25	9.06	8.27	13.97
Contributed Equity	21.95	32.61	41.16	41.16	41.16	41.16	41.16
Retained earnings	-21.37	-24.00	-26.63	-29.03	-31.19	-32.07	-26.57
Reserves	-0.21	-0.21	-0.21	-0.21	-0.21	-0.21	-0.21
NCI	-0.04	-0.34	-0.55	-0.67	-0.70	-0.61	-0.41
Total equity	0.34	8.06	13.77	11.25	9.06	8.27	13.97

Statement of Cashflows *A$'000s*	CY24	CY25	CY26	CY27	CY28	CY29	CY30
Net profit for period	-2.85	-2.94	-2.60	-2.28	-0.92	5.60	15.60
Depreciation & Amortisation	0.11	0.95	0.97	0.99	0.87	0.96	1.98
Changes in working capital	0.28	-0.27	-0.67	-1.30	-4.16	-6.21	-3.39
Other	-0.05	-0.06	-0.09	-0.13	-0.20	-0.30	-0.54
Operating cash flow	-1.84	-2.32	-2.39	-2.72	-4.41	0.05	13.65
Payments for PPE	-	-0.01	-0.01	-0.01	-0.01	-	-
Loan receivable	-0.26	-	-	-	-	-	-
Other	-	-0.05	-0.00	-0.01	-0.00	-0.00	-0.00
Investing cash flow	-0.26	-2.86	-2.87	-2.93	-2.57	-2.81	-5.90
Equity Raised	2.08	11.22	9.00	-	-	-	-
Transaction costs	0.40	-0.56	-0.45	-	-	-	-
Borrowings	-	-0.12	-	-	-	-	-
Proceeds from exercise of options	-	0.30	1.76	3.51	2.28	0.30	0.18
Other	0.04	-	0.26	-	-	0.00	0.00
Financing cash flow	2.53	10.84	10.57	3.51	2.28	0.30	0.18
Free cash flow	**-5.18**	**-5.26**	**-5.65**	**-6.98**	**-2.75**	**7.75**	**45.09**
Cash flows	**5.66**	**5.31**	**-2.14**	**-4.70**	**-2.45**	**7.92**	**26.44**
Effects of exchange rate	-	-	-	-	-	-	-
Cash year end	6.16	11.46	9.33	4.63	2.17	10.10	36.54

Investment Fundamentals	CY24	CY25e	CY26e	CY27e	CY28e	CY29e	CY30e
Liquidity							
Quick Ratio	0.5	0.2	0.2	0.2	0.2	0.2	0.3
Solvency							
Debt to Equity	1.0	0.0	0.0	0.0	0.0	0.0	0.0
Debt to Assets	0.3	0.0	0.0	0.0	0.0	0.0	0.0
LT Debt to Assets	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Profitability							
Net Margin	n/a	n/a	n/a	n/a	n/a	23%	32%
ROA	-310%	-51%	-19%	-12%	-4%	17%	30%
ROE	-2487%	-63%	-22%	-17%	-9%	64%	138%
Profit Margins							
EBITDA Margin	n/a	n/a	n/a	n/a	n/a	23%	30%
Gross Margin	58%	59%	60%	61%	62%	62%	62%
NPAT Margin	n/a	n/a	n/a	n/a	n/a	15%	20%

Exchange differences on translation were not considered in the overall OCI assessment, as they result from marginal foreign currency translation differences that do not materially impact the financial outlook.

Board & Management

Dr David Pevcic Executive Chairman	Appointed Executive Chairman in 2024, Dr David Pevcic brings a strong background in investment and corporate strategy across the technology and resources sectors. He currently serves as Executive Director of Infini Resources (ASX:I88) and Non-Executive Director of Battery Age Minerals (ASX:BM8). Dr Pevcic is also the founder of several private ventures and holds degrees in Science and Medicine from the University of Western Australia.
Alfred Chong Group Chief Executive Officer	Founder of Nanoveu, Alfred Chong has over 30 years of experience scaling technology businesses across the US and Asia. Prior to Nanoveu, he held senior executive roles including CEO of THISS Technologies and 121View, and CMO at 3D International. Recognised by the Singapore American Business Association and *San Francisco Chronicle* as a key innovator, Chong holds degrees in Computer Science and an MBA from the University of San Francisco.
Steve Apedaile Non-Executive Director	With over three decades in accounting and corporate finance, Steve Apedaile has held senior positions at KPMG and Horwath in Hong Kong. He is a former MD of an ASX-listed company and brings deep expertise in international business and forensic accounting. Apedaile is a Fellow of the UK Institute of Chartered Accountants and a member of the AICD.
Dr Michael Winlo Non-Executive Director	Dr Winlo has led teams in biotech, pharma, and big data, including as CEO of Linear Clinical Research and health lead at Palantir Technologies (Silicon Valley). He is currently Executive Director of Emyria (ASX:EMD). Dr Winlo holds an MBA from Stanford and medical degrees from the University of Western Australia.
Mark Goranson CEO Semiconductor Technology	Mark Goranson leads Nanoveu's chip commercialisation with over 25 years in the semiconductor industry, including 18 years at Intel and roles at ON Semiconductor, Freescale, and TE Connectivity. His background spans chip manufacturing, productisation, and strategic scaling. He holds a BSc in Physics/Electronics from New Mexico University.
Mohamed M. Sabry Founder of EMASS	Prof. Sabry is a leading voice in embedded AI and chip design. A former Associate Professor at NTU Singapore and postdoc at Stanford, he founded EMASS and has led major government-backed deep tech programs. His research includes over 100 peer-reviewed publications and over S$40 million in secured funding.
Raymond Chen Group CFO	Raymond Chen has held senior finance roles at Iluka, NRW Holdings, Equinox, and KPMG. His responsibilities included IR, treasury, and capital markets. He holds an MBA from the University of Cambridge's Judge Business School.

Evolution Capital Ratings System

Recommendation Structure	• **Buy:** The stock is expected to generate a total return of >10% over a 12-month horizon. For stocks classified as 'Speculative', a total return of >30% is expected. • **Hold:** The stock is expected to generate a total return between -10% and +10% over a 12-month horizon. • **Sell:** The stock is expected to generate a total return of <-10% over a 12-month horizon.
Risk Qualifier	• **Speculative:** This qualifier is applied to stocks that bear significantly above-average risk. These can be pre-cash flow companies with nil or prospective operations, companies with only forecast cash flows, and/or those with a stressed balance sheet. Investments in these stocks may carry a high level of capital risk and the potential for material loss.
Other Ratings:	• **Under Review (UR):** The rating and price target have been temporarily suppressed due to market events or other short-term reasons to allow the analyst to more fully consider their view. • **Suspended (S):** Coverage of the stock has been suspended due to market events or other reasons that make coverage impracticable. The previous rating and price target should no longer be relied upon. • **Not Covered (NC):** Evolution Capital does not cover this company and provides no investment view.

Expected total return represents the upside or downside differential between the current share price and the price target, plus the expected next 12-month dividend yield for the company. Price targets are based on a 12-month time frame.

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